

## Designing Robust Microcontrollers for Debugging After Silicon

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Paper received: 2025/03/01, Paper accepted: 2025/06/13

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**Abstract:** Post-silicon debugging is a critical phase in the development of microcontrollers, where latent design bugs, signal integrity issues, and timing violations often emerge that were not detectable during pre-silicon verification. This paper presents a comprehensive approach to designing robust microcontrollers with built-in debug capabilities to streamline post-silicon validation and failure analysis. We explore architectural enhancements such as embedded trace buffers, hardware breakpoints, scan chains, and real-time observability features that facilitate detailed monitoring and control without significantly impacting area or performance. Furthermore, we discuss methodologies to ensure minimal debug overhead and propose a scalable debug framework that supports rapid root cause analysis across varying use cases. The proposed design strategies aim to reduce time-to-market, improve first-pass silicon success rates, and enhance the overall reliability of embedded systems.

**Keywords:**

Post-silicon debugging, Microcontroller architecture, Embedded trace, Real-time observability, Hardware breakpoints

**Introduction**

The increasing complexity of microcontroller units (MCUs) in modern electronic systems has intensified the need for robust debugging techniques, especially during the post-silicon phase. While pre-silicon verification, including simulation and formal verification, is critical for identifying functional errors and design flaws, it cannot guarantee complete correctness due to limitations in test coverage and modeling abstraction. Consequently, some defects only surface after the silicon has been manufactured. These post-silicon bugs can include timing violations, hardware/software integration failures, signal integrity issues, or errors resulting from process variation and environmental conditions. The high cost and time implications of silicon respins make it imperative to adopt effective strategies for observing, diagnosing, and rectifying post-silicon anomalies efficiently.

Designing microcontrollers with robust debug capabilities from the ground up ensures that system integrators and chip designers have access to deep insights into internal signals, execution flows, and real-time performance. Debug features like trace modules, hardware breakpoints, on-chip

debug ports, scan chains, and built-in self-test (BIST) mechanisms are indispensable tools. However, embedding these capabilities poses its own set of challenges, such as area overhead, increased power consumption, and potential security vulnerabilities. This necessitates a balanced design that integrates comprehensive debug functionality without compromising the MCU's performance or cost targets.

This paper explores architectural methodologies and hardware instrumentation techniques that enhance the observability and controllability of microcontrollers during post-silicon validation. We focus on designing MCUs that can expose internal states without external probing, facilitate rapid root cause analysis, and support iterative debugging workflows in real-world applications. By doing so, we aim to provide a scalable framework for enabling faster time-to-market and higher reliability in embedded systems.

## Literature Review

Post-silicon validation has been the subject of extensive research due to its significant role in the hardware design lifecycle. Agarwal et al. (2013) emphasized the “design-for-debug” (DfD) paradigm, advocating the integration of debug logic during early design stages to reduce time and cost in post-silicon diagnosis. Their work laid the foundation for embedding visibility mechanisms like trace buffers and logic analyzers directly into silicon. In a similar vein, Sun et al. (2016) investigated trace compression schemes for post-silicon debug, showing that efficient compression of trace data can alleviate memory bandwidth and storage limitations while preserving crucial information for analysis.

Work by Mitra and McCluskey (2005) introduced the concept of scan-based debugging, which enabled fine-grained observability and fault localization using scan chains and flip-flop instrumentation. This approach was further enhanced by modular debug infrastructure, where blocks of logic were independently instrumented and debugged. These methods, while effective, introduced area and power overheads that made them less suitable for cost-sensitive MCU designs. To address this, Zhang et al. (2018) explored lightweight debug circuitry using reconfigurable logic and shadow registers, significantly reducing hardware overhead while maintaining adequate debug visibility.

The evolution of multicore microcontrollers and mixed-signal SoCs has also influenced debug methodologies. According to Bosch and Freescale (2014), automotive-grade microcontrollers now demand real-time in-system trace and deterministic replay capabilities, especially for safety-critical applications compliant with ISO 26262 standards. Consequently, debug architectures have shifted towards hierarchical trace systems, deterministic recorders, and non-intrusive sampling mechanisms. Moreover, ARM's CoreSight and RISC-V's Nexus-like debug specifications illustrate how standardized debug interfaces are becoming integral parts of MCU ecosystems.

Recent studies have also explored AI-assisted post-silicon debugging. Research by Rao et al. (2023) demonstrated how machine learning models trained on pre-silicon simulation data could

predict probable bug locations during post-silicon validation, significantly accelerating the debug cycle. These data-driven approaches, combined with hardware instrumentation, represent a hybrid model for future-proof debugging.

Despite these advancements, challenges remain in achieving minimal latency, low-cost, and high-resolution debug architectures suitable for diverse MCU applications — from consumer electronics to industrial automation and autonomous systems. This paper builds upon the existing body of research by proposing novel architectural and design optimizations that enhance debug robustness while adhering to the constraints of embedded microcontroller platforms.

## Methodology

The methodology of this research involves the design, integration, and evaluation of a debug-optimized microcontroller architecture intended to enhance post-silicon observability and control. Our approach combines architectural innovation, simulation modeling, and hardware prototyping to validate the effectiveness of the proposed debug features.

### 1. Design-for-Debug (DfD) Framework

The first step involved outlining a comprehensive DfD framework tailored for resource-constrained microcontroller environments. The framework emphasized:

- **Internal Signal Observability:** Embedding trace logic and debug ports to access internal registers, buses, and ALU operations.
- **Real-time Debug Interfaces:** Inclusion of Serial Wire Debug (SWD), JTAG, and trace modules that could output program counter and event data during execution.
- **Trigger-Based Capture Logic:** Implementation of event-driven capture systems that log execution behavior based on user-defined breakpoints, watchpoints, or error flags.
- **Timestamped Trace Buffers:** Integration of circular buffers to store timestamped trace data for precise post-mortem analysis.

### 2. Instrumentation Modules

Instrumentation components were developed as modular RTL blocks in Verilog and SystemVerilog and included:

- **Embedded Trace Macrocell (ETM):** Captures instruction-level execution traces without halting the core.
- **Trace and Debug Memory Controller (TDMC):** A memory controller capable of offloading trace data to external RAM or internal non-volatile memory.
- **Scan Chains and Shadow Registers:** Added to critical logic paths to enable visibility of internal states during scan-based testing.

- **Built-In Self-Test (BIST):** Lightweight self-testing logic for memory and logic units, ensuring test coverage in edge cases.

### 3. Simulation and Pre-Silicon Verification

The DfD architecture was validated in pre-silicon simulation using Synopsys VCS and Cadence Xcelium environments. Testbenches were developed to stimulate typical microcontroller tasks (e.g., I/O toggling, timer operations, interrupt handling) and capture debug trace output under both normal and fault-injected scenarios.

- **Fault Injection:** Timing glitches, stuck-at faults, and memory access errors were introduced to evaluate the debug features' detection accuracy.
- **Power and Area Estimation:** Power estimation was performed using Synopsys PrimeTime PX, while area overhead was analyzed via synthesis with Design Compiler.

### 4. Prototype Development and Post-Silicon Validation

An FPGA-based prototype was developed using Xilinx Zynq-7000 SoC to emulate the microcontroller with debug logic. The design was ported onto the FPGA using Vivado, enabling real-time debug interface testing with external tools (e.g., OpenOCD, Lauterbach TRACE32).

- **Use Cases Tested:**
  - Memory corruption during DMA transfer
  - Interrupt latency tracking
  - Execution path divergence due to branch prediction
- **Debug Interface Evaluation:**
  - Latency of data capture
  - Resolution of internal signal visibility
  - Non-intrusiveness during real-time operation

## Results

The evaluation of the proposed debug-optimized microcontroller architecture yielded the following results across observability, accuracy, performance, and overhead metrics.

### 1. Enhanced Observability

- **Instruction Trace Coverage:** The embedded trace module captured >95% of all instruction-level transitions over a 10,000-cycle test window.
- **Signal Visibility:** Internal buses and critical registers were visible at a resolution of one clock cycle, enabling precise root cause analysis during fault events.

- **Real-Time Logging:** Using circular trace buffers, execution logs with timestamp precision of  $\pm 1$  cycle were obtained during runtime.

## 2. Debug Accuracy and Fault Localization

- **Detection of Timing Violations:** All injected timing-related faults (N=20) were accurately identified using edge-sensitive trigger logic and waveform reconstruction from trace logs.
- **Root Cause Resolution Time:** Average time to locate faults using the debug system was reduced from ~9 hours (manual probing) to under 1.5 hours.
- **Breakpoints and Watchpoints:** Hardware-supported breakpoints worked with 100% accuracy, and memory watchpoints detected >98% of target events across multiple use cases.

## 3. Performance Impact

- **Execution Overhead:** The real-time trace system introduced <3% latency during high-frequency operation (100 MHz core clock), with negligible effects on application execution.
- **Debug Interface Throughput:** Serial debug interfaces sustained data rates up to 3 Mbps (SWD) and 10 Mbps (JTAG), sufficient for low to medium complexity MCU applications.

## 4. Resource Utilization and Overhead

- **Area Overhead:** Synthesis results showed that debug logic consumed approximately 9% additional gate count over the baseline MCU design (measured across a 32-bit RISC-V core).
- **Power Consumption:** Estimated increase in dynamic power was 5.7% during active debug sessions. When disabled, power overhead was negligible due to clock gating of debug blocks.
- **Security Trade-offs:** Although the debug interface was vulnerable to unauthorized access, secure debug lock mechanisms and encrypted authentication protocols mitigated risk.

## 5. Comparison with Industry Baselines

Feature	Proposed Design	ARM Cortex-M3 ETM	Open-Source RISC-V Debug
Trace Coverage	95%	91%	85%
Breakpoint Support	4 hardware slots	2 hardware slots	1 hardware + 1 software
Real-time Performance Impact	<3%	~5%	~7%
Area Overhead	+9%	+12%	+8%

Time to Debug a Fault (avg.)	1.4 hrs	2.5 hrs	4 hrs
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These results validate the effectiveness of integrating a structured, hardware-assisted debug framework into microcontroller designs. The proposed methodology significantly improves debugging efficiency after silicon, while balancing performance, power, and cost trade-offs.

## Discussion

The results of our evaluation demonstrate that incorporating structured, hardware-assisted debugging capabilities into microcontroller architectures significantly improves the effectiveness of post-silicon validation. One of the key takeaways is the ability to observe internal states with high fidelity in real time, which is often a limitation in traditional post-silicon debug environments. The proposed solution—featuring trace modules, embedded debug ports, scan chains, and breakpoint logic—provides a comprehensive toolset that can isolate timing and logic faults more efficiently than software-only or external probing techniques.

A major advantage of our design lies in its minimal performance and power overhead. By leveraging clock gating and modular debug logic activation, we ensured that debug features remained non-intrusive during standard operation. The area overhead of 9% is an acceptable trade-off, especially when weighed against the time savings during root cause analysis and fault isolation. Furthermore, our system’s fault localization capabilities, enabled by precise timestamped trace logs and event-driven capture, drastically reduced the mean time to debug complex hardware/software interaction failures.

One challenge that emerged during implementation was the integration of debug logic with security features. In applications such as automotive or industrial automation, unauthorized access to debug interfaces could result in significant vulnerabilities. We addressed this by incorporating authentication and secure debug lock mechanisms, although this area requires further research, particularly as microcontrollers become increasingly deployed in safety-critical environments.

Additionally, the adaptability of our debug framework across different MCU configurations—ranging from single-core to multicore and from general-purpose to real-time applications—highlights its scalability. As microcontroller-based systems evolve with added complexity (e.g., machine learning accelerators, secure enclaves), the importance of robust, flexible debug infrastructure will only increase.

This work aligns with emerging trends in industry, such as the adoption of open-standard debug interfaces (like RISC-V Debug Specification and ARM’s CoreSight), and provides a forward-compatible blueprint for extending debug capabilities with minimal overhead. The combination of classical debug techniques with modern trace compression and intelligent trigger logic opens pathways for future integration of AI-driven fault prediction models directly on-chip.

## Conclusion

This paper presented a comprehensive methodology for designing microcontrollers with enhanced post-silicon debug capabilities. By embedding real-time observability, trace capture logic, and scan-based instrumentation into the MCU architecture, we enabled high-resolution debugging with minimal performance degradation. Through simulation and hardware prototyping, we demonstrated the effectiveness of our framework in detecting, localizing, and resolving post-silicon bugs faster and more accurately than traditional approaches. Our approach provides an essential step forward in closing the observability gap between pre- and post-silicon verification phases. The proposed framework supports rapid debugging, enhances reliability, and accelerates time-to-market—critical factors in the competitive semiconductor landscape. Future work will explore dynamic reconfiguration of debug logic and integration with machine learning-based anomaly detection engines to further automate and streamline post-silicon debugging processes.

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